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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/023,235	BERNSTEIN ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-40 has/have been presented for examination based on amendment filed on 15th August 2006. This action is in response to the request for continued examination filed on 22nd September 2006.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15th August 2006 has been entered.
3. Claim(s) 1-9, 13-14, 19, 24, 30, 36-40 is/are amended.
4. The arguments submitted by the applicant have been fully considered. Claims 1-40 remain rejected. The examiner's response is as follows.
5. Previous rejection to claims 1-40 under 35 USC 103 are withdrawn and new rejections are made upon further review of the references based on the amendment and arguments.

Claim Interpretation

Regarding Claim 1

6. The phrase "performance parameter" is understood as the current voltage switch-point of a transistor computer model in reference to claim and as understood from specification [0018].

7. The phrase "first bounded range" is a range representing the variation in the "performance parameter" due to variation in the single manufacturing process. In other words, first bounded range represents a range of current voltage switch points of a transistor computer model due to variations in the single manufacturing process.

8. The phrase "second bounded range" is a range representing the variation in the "performance parameter" due to variation in the design of device. In other words, second bounded range represents a range of current voltage switch points of a transistor computer model due to variations in designs of a transistor. For example variations in design of transistor is understood as change in length & width of transistor.

Regarding Claim 19

9. The "primary parameters" of a feature as disclosed in the specification ([0039]) are performance characteristics that are directly related to the specific physical feature. For example, in MOSFET designs, the overlap capacitance (C.sub.ov) is directly related to the length of the physical overlap of the gate material over the diffusion and extension (or lightly-doped drain) implants and the gate oxide thickness.

10. The "secondary parameters" of a feature, as disclosed in the specification ([0040]-[0041]) are calculated based on the one or more primary parameters. Fir example total gate capacitance.

Response to Applicant's Remarks & Examiner's Withdrawals

11. Applicant's remarks regarding Premature Final are considered and are moot in view of the request for continued examination.

12. Applicant's remarks regarding claim 23, 28 and 29 are also moot in view of request for continued examination.

Response to Applicant's Remarks

13. **Claims 1-27 & 30-40 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hershenson (HE'277), in view of Krivokapic (KR'527).**

Regarding Claim 1

Applicant argues that Krivokapic (KR'527) does not discuss the "range bounds" and since the invention is complex the particular piece should be clearly explained. Examiner has states that "range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63). "Range bounds" are taught in the cited portion as "guard bands" in the I/V curves and this cited portion would have been obvious to one designing I/V characteristics of the integrated circuit where the bounds of the I/V curves are assessed for worst case scenarios. Therefore examiner respectfully disagrees with applicant's argument that Krivokapic (KR'527) does not discuss the "range bounds".

Regarding Claim 9

Applicant has argued that claim 9 recites a "computer implemented method that comprises a designing step using a computer model that is created using a given target performance parameter of a given performance attribute", a feature not included in the "simulator" of independent claim 1. Examiner had rejected claim 9 on

the similar basis as claim 1. Since the references are complex, this feature is not clearly shown.

Examiner respectfully disagrees that these limitations are not similar and asserts that they are taught by the same reference (HE'277: Col.4 Lines 61-67 - designing the model; Col.3 Line 67 - Col.4 Line 5 - performance parameter). It is well known to one of ordinary skill in the art of simulation that simulation of integrated circuit models is used design integrated circuits. The step of designing the model has to present when the model is being simulated. Examiner finds the applicant's unpersuasive.

Response to Applicant's Remarks for Objections

14. Claim 33 was objected to for improperly being dependent on claim 30 and further not limiting the limitations presented in claim 30. Examiner notes that Applicant has amended claim 30 to cure the deficiency and the objection is withdrawn.

Response to Applicant's Remarks for 35 USC 112, second paragraph

15. Regarding Claim 14-24

Applicant has stated examiner's previous rejection and attempted to clarify the distinction between the "product" and "device".

Firstly, Applicant has pointed out to specification paragraph [0017], where as the text of the specification paragraph [0015] is cited there according to specification submitted to the office on 17th December 2001.

Secondly, specification states "that this invention is also applicable to any component of any product, where the performance attributes of that component help determine the functionality of the integrated product." This statement states the obvious and most general feature of anything that has sub constituents making that thing.

It seems like all the arguments referring to specification are offset by at least 2 paragraphs hence they do not seem coherent with the arguments presented. Although the arguments are considered, they are not found to be persuasive as it cannot be ascertained which paragraph of specification they are pointing towards. A corrected argument may be found persuasive.

New rejection is made further based on the claim language for distinction between the "product" and "device". Please see 35 USC 112 section below.

Regarding Claim 36 and 40

Previous rejection is withdrawn in view of the amendment and arguments, however new rejection is presented. Please see 35 USC 112 section below.

Response to Applicant's Remarks for 35 USC 101

16. **Claims 1-8, 36-40 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

Regarding Claim 1-8

Rejection is withdrawn in view of claim amendment including limitation that discloses the simulator as a tangible product (having memory and processor) and not software per se in claim 1.

Regarding Claim 36-40

Claims 36-40 are amended to include "storage device" which as read from specification ([0047]) include disk or tape units having executable model being executed by a computer. Rejection is withdrawn.

Response to Applicant's Remarks for 35 USC 103

17. **Claims 1-27 & 30-40 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hershenson (HE'277), in view of Krivokapic (KR'527).**

Regarding Claim 1, 9, 14, 19, 24, 36 and 40

Applicant has alleged that the Hershenson's teaches designing integrated circuit in a manner different from the present invention.

Examiner respectfully disagrees as HE'277& KR'527 teach the limitations presented in the claims. Please see updated claim rejections in view of claim interpretation.

(Argument 1) Applicant has argued that the inequality constraints presented do not amount to a first bounded range or a second bonded range of a performance parameter o a single component device (e.g. transistor etc).

(Response 1) Examiner has reconsidered the teaching of HE'277& KR'527 and applicant's arguments to clarify the ambiguity regarding claim interpretation of first bounded range or a second bonded range to update the rejection.

(Argument 2) Applicant has argued that multiple designs refer to multiple design single component (i.e. transistor).

(Response 2) Examiner thanks applicant for clarification, HE'277 teaches variation of a single design (HE'277: Col.5 Lines 40-48).

(Argument 3) Applicant argues that nowhere in the cited portion of KR'527 are "range bounds" for a target performance parameters are disclosed. But argues to the contrary the following:

> Thus, Krivokapic discloses an improved method for modeling in which The I/V curves that are obtained are used to show how choice of semiconductor device attributes, such as channel length, effect the guard band or manufacturability of such devices (see col. 4, lines 25-34).

(Response 3) Applicant has presented evidence contrary to argued to point, buttressing examiner's argument. Please see claim interpretation section for interpretation of different bound ranges. Further, KR'527 Fig.6a-c show a simulator with feedback of the bound ranges (Element 642- I/V Device store) based on the performance parameters (M (L, T, N)).

(Argument 4) Applicant has indicated that even if for sake of argument above interpretation and examiner's conclusion accepted, KR'527 does not teach first bound range of a target performance parameter for a performance attribute, where the performance parameter variation occurs within a single manufacturing process.

(Response 4) Examiner is unclear how the applicant is reaching this conclusion. KR'527 clearly teaches Process variations as PS1-PSn (Fig.6a Element 605; Col.11 Lines 19-56). Also see KR'527 Col.13 Lines 40-62 as follows:

> The calibrated current values are then output on line 670 to statistical analyzer 646. Statistical analyzer 646 creates a mean I.sub.R and standard deviation .sigma.I.sub.R associated with each of the drain-to-source voltage values V.sub.1, V.sub.2, V.sub.3 . . . V.sub.R and outputs the results on line 647 to statistical distribution store 650. Statistical distribution store 650 includes a Table 650a having corresponding mean I.sub.R and standard deviation current values .sigma.I.sub.R corresponding to the R drain-to-source voltage values. In an alternate embodiment, a smallest (or 2nd smallest) and largest (or 2nd largest) current maximum could be used for statistical guard bands. Based upon the mean current and standard deviation values in Table 650a, worst-case I/V curves 651a and 651c may be constructed along with an idealized I/V curve 651b. Manufacturing guard bands 651d and 65le then may be determined based upon the difference between idealized I/V curve 651b (consisting of mean I.sub.R values) and worst-case curves 651a and 651c. The curves 651a and 651c

> consist of positive and negative 3 .sigma.I.sub.R values. Moreover, probabilities may be assigned to various curves constructed within the worst-case curves to identify manufactured guard bands. A parameter extractor device and software then may be used to obtain parameters associated with curves 651, 651a and 651c.

The ranges as indicated are obtained though simulation and actual results. The claimed limitations do not specify how the ranges are determined, hence the argument that the I/V curves are obtained from the modeling not used to create a model. As taught above by KR'527 the parameter extractor uses these ranges to compute the parameters for the model for simulation.

The limitations disclosed will be mapped for brevity and clarity. Please see updated rejection.

Applicant's arguments are found to be unpersuasive regarding the discussed claims and the rejection is maintained.

Regarding Claim 1, 24 and 40

(Argument 5) Applicant has argued that HE'277 does not teach a model for and IC (product) that is based on a target model (based on performance parameter for a given device –e.g. transistor), but rather discloses a transistor model and performance specification of a multi-component device.

(Response 5) Since the claimed product has only one device (e.g. chip/IC with one transistor), the performance goal for the product and device seem to be the same. Examiner agrees that teaching provided by HE'277 is much more complex, however it encompasses the claimed limitation of "a product having a device", or a design having a transistor. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), See also In re Larson, 340 F.2d 965, 144 USPQ 347 (CCPA 1965).

Regarding Claim 19

Applicant has argued the distinction between the first bounded range, second bounded range, primary and secondary parameters. Examiner has noted the argument and updated the rejection with claim interpretation for each of the terms. Rejection for the claim is maintained.

Regarding Claim 23

Applicant has argued that prior art, KR'527, does not disclose "determining asset of design distributions that are within a given set of performance targets for a plurality of parameters" and determining whether an altered design is within "said set of design distributions".

Examiner respectfully disagrees; constraints specified are the given set of performance targets for a plurality of parameters, where the optimization based on that yields design distributions for various levels of optimizations (i.e. determining which design will be suitable for a given level op optimization).

Examiner's Response to Motivation to Combine

MPEP 2143.01 Suggestion or Motivation To Modify the References first recites:

> "There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998)

Nature of problem to be solved: The problem to be solved is determining & establishing the parameters affecting the device design (e.g. transistor) based on the process and design variations. HE'277 is a simulator which models both process and design variations (HE'277: Col.5 Lines 27-35; Col.6 Lines 1-48; Col.20 Lines 6-21, Col.21 Lines 10-34; Col.5 Lines 40-48). KR'527 is a simulator for process and design variation simulator connected to an actual manufacturing process (KR'527: Fig.6a). The teaching of HE'277 simulator using geometric programming are advantageous over the simulator disclosed in the KR'527 as disclosed by HE'277 as geometric programming quickly generates globally optimal designs for wide range of performance specification (like process and design variations) (HE'277: Col.3 Lines 9-59).

Teachings of the prior art & knowledge of persons of ordinary skill in the art: Both HE'277 and KR'527 show various softwares that would be known to one skilled in the art to commensurate such modeling task. HE'277 teaches various CAD tools including TILOS (HE'277: Col.1 Line 37-Col.3 Line 59). KR'527 teaches various device simulators like PISCES, MINIMOS and process simulator like DEPICT.

Further by applicant's own admission such modeling softwares as FIELDAY, or DAMOCLES are also known in the art (Specification: [0033]). Applicant's arguments are found to unpersuasive.

Claim Rejections - 35 USC § 112, first paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

18. Claim 1-40 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The "second bounded range" identifying the variation between multiple design is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Claims 1, 9, 14, 19, 24, 36 and 40 disclose second bounded range representing the performance parameter variations between multiple designs. The figure 1 & 2 and accompanying disclosure do not teach how the second bounded range would be bounded between multiple designs. Further, there is no disclosure of multiple design of a transistor, a resistor or a capacitor thereby identifying various models.

19. Claim 1-40 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The "capacitor" or "resistor" models amended in the claim do not have disclosed support for performance parameter like the transistor model, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

The transistor model has "current voltage switch point" (Specification: [0018]) as support for the "performance parameter" where as there is no such disclosed

relevant support for "performance parameter" of resistor or capacitor model is disclosed. One skilled in the art cannot infer that "current voltage switch point" as performance parameter is also applicable to the capacitor or resistor model. As commonly known in the art transistor model and resistor/ capacitor model have different attributes and behavior from each other and their performance parameters are not same. No such disclosure is present in the specification for these models.

20. Claim 1-40 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Claims disclose generating computer model based on a target model where the target model is created using the performance parameters – the disclosure lacks enablement for creating such a computer model effectively based on performance parameters, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

21. Claim 1-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1-40

Independent claims 1, 9, 14, 19, 24, 36 and 40 disclose limitation "first bound range" and "second bound range" for a "performance parameter". However no specific ranges are provided for this claim thereby failing to provide for the metes and bound for the ranges.

Further it is unclear from the claim language if the first bounded range or a second bonded range are computer in same simulation, i.e., if the process and design performance parameters are varied at the same time during the simulation.

Regarding Claim 14 & 24

Claims disclose a "*A method of developing **a product** having **a device** with at least one performance attribute, wherein the said device is one of a transistor, a capacitor and a resistor, said method comprising:*".

From the language it seems that ***a product*** has only ***a (one) device*** and the product and device are equivalent for all intensive purposes. Further limitations indicating distinction between the "a product" and "a device" are moot. E.g. newly amended limitation "*developing device goals for said device, wherein said device goals are*

*based on **[antecedent basis]** product goals*", or "designing said product with said device based on said target model".

Regarding Claim 23

Applicant has argued the limitation "set of design distributions". Examiner believes that the rejection is well within the scope of the claim. However the arguments presented seem unclear in view of rejection. Clarification for limitation "set of design distributions" is requested.

Regarding Claim 36

Amended preamble in claim 36 discloses a rather confusing language. As stated, it is unclear, which subject each "that" (repeated three times in preamble) refers to in the preamble.

> "A program storage device readable by computer and tangibly embodying a model of an integrated circuit device ***that*** has at least one performance attribute, ***that*** is one of a transistor, a capacitor and a resistor, and ***that*** is executable by said computer, said model comprising:"

22. **Claim 14 recites the limitation "product goals". There is insufficient antecedent basis for this limitation in the claim.**

Regarding Claim 14

The limitation is stated as

> "developing device goals for said device, wherein said device goals are based on **[missing antecedent basis]** product goals".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

23. Claims 1-27 & 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277hereafter) in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of applicant's own admission.

Regarding Claim 1

HE'277 *teaches a simulator* (HE'277: Col.4 Lines 61-Col.5 Line 6) *comprising: a memory for storing a computer model of an integrated circuit comprising a device that is one of a transistor* (HE'277: Col.6 Lines 58-62) *and has at least one performance attribute* (HE'277: Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15); *wherein the said computer model is generated based on the target model for said transistor* (HE'277: Col.6 Lines 58-62) *and wherein said target model is create using performance parameter for the said performance attribute* (HE'277: Col.5 Lines 40-46). The transistor models are posynomial models, which are created (optimized) for one or more performance specifications (HE'277: Col.6 Lines 3-6). HE'277 further teaches, said target model *is adapted to predict process and design variations of said device* (HE'277: Col.5 Lines 27-35; Col.6 Lines 1-48). HE'277 teaches *a processor in communication with the said memory device and adapted to execute said computer model* (HE'277: Col.4 Lines 61-Col.5 Line 6; Col.6 Lines 58-67). HE'277 teaches *target performance parameter includes a first bounded range* (due to process variation being modeled as inequalities - HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34) *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277:

Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches *said first bounded range comprises performance parameters variations within the single manufacturing process based on a single design for said device* (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34 & 41-60) and; HE'277 teaches said second bounded range *comprises performance parameters variations between designs for said design device (*HE'277: Col.11 Lines 40-Col.12 Line16) as variations in at least the Length and Width of the transistor.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process *where the performance parameter are current voltage switch point (See claim interpretation)*, although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example, **as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 2

HE'277 teaches that *multiple* designs are directed to variations of a single *design* (HE'277: Col.11 Lines 40-Col.12 Line16). For example changing the width (W) and lengths (L) of the transistors.

Regarding Claim 3

HE'277 does not explicitly teach performance parameter is the same for a *target* model of said device and a final hardware design of said device as the (performance) parameters are used for manufacturing and modeling. HE'277 also does not teaches interaction between the actual manufacturing and model simulation.

KR'527 teaches that performance parameter is the same for a *target* model of said device and a final hardware design of said device (KR'527: Fig.6a, Fig.3) as the (performance) parameters are used for manufacturing and modeling. KR'527 teaches in interaction between the actual manufacturing and model simulation (KR'527: Col.9-11).

Regarding Claim 4-7

HE'277 teaches using multiple constraints where the constraints vary as defined in the simulation, further HE'277 teaches performing tradeoff optimization between various constraints graphically displayed as curves (HE'277: Col.6 Lines 3-24). KR'527 also teaches statistical Monte Carlo based inputs (as ranges) & range correction (KR'527: Fig.6b, Col.12 Lines 8-50). Plurality of performance points are selected as various input parameter values from statistical distributions mentioned above.

Regarding Claim 8

HE'277 teaches using geometric programming with its advantageous ability to solve thousands of constraints (HE'277: Col.5 Lines 6-35). Further, HE'277 teaches these

constraints can be displayed as tradeoff (implying at least two constraints with plurality of evaluated results) in form of curve representing *target* performance parameters with two-dimensional range of plurality of performance points (HE'277: Col.6 Lines 3-24; Also see KR'527: Col.12 Line 63-Col.13 Line 23).

Regarding Claim 9

Method claim 9 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 10

Method claim 10 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 11

Method claim 11 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 12

Method claim 12 discloses similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 13

Method claim 13 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 14 & 15 (Updated)

Method claims 14 & 15 disclose similar limitations as claim 1 and are rejected for the same reasons as claim 1. Limitation disclosed as "design goals" is further disclosed

as "performance parameter". HE'277 teaches producing a target model (HE'277: Col.4 Lines 61-67). *Further, KR'527 teaches developing a device and product based on the target model (KR'527: Fig.6a, Col.9-11 Section III). The goals for device and product are interpreted as same goal, as indicated in the preamble "a product having a device" shows that product only has one device.* KR'527 teaches target performance comprises plurality of performance points as points in the V/I curves (KR'527: Fig. 6c). *Further by applicant's disclosure, the tools to predict process and design variations are known in the art (Specification: [0033]).*

Regarding Claim 16

Method claim 16 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 17

Method claim 17 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 18

Method claim 18 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 19 (Updated)

Method claim 19 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. KR'527 teaches developing a design for the device based on the target model (in simulator) (KR'527: Fig. 6a). KR'527 further teaches modifications to design wherein modification comprises modifying a particular feature and adding a

particular feature of the design (KR'527: Col.6 Lines 34-59). KR'527 teaches determining primary parameters for a particular feature; determining secondary parameters from the said primary parameters (KR'527: at least in Col.2 Lines 51-63; also in Fig.6a-b-c- element 680-615-618; Col.13 Lines 10-23 – I/V curve from L, T, N parameters).

KR'527: Col.2 Lines 51-63 states:

> Before an accurate model of semiconductor device 200 may be obtained, certain "parameters" must be extracted from semiconductor device 200, as illustrated in FIG. 1. Typically, a device simulator requires specific device "parameters" in order to provide a simulation. For example, one semiconductor device simulator requires five specific sets of parameters, as illustrated by parameters 103-107. Some of the parameters are extracted from device parameter extractor 102. Some of these parameters may correspond to physical measurements of transistor device 200, such as channel length L and doping concentration N+ ***[Primary parameters]***, while other parameters may be based on or derived from these physical measurements or other parameters ***[secondary parameters]***.

KR'527 teaches determining secondary parameters from said primary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 – I/V curve from L, T, N parameters) where the primary parameters are inputted into process simulator and secondary parameters are derived from primary parameters (element 680-615-618) and inputted into device simulator (Element 640).

KR'527 teaches balancing choices (KR'527: Col.2 Lines 20-24, Col.4 Lines 30-34) related to modification and particularly to primary and secondary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 – I/V curve from L, T, N parameters; element 680-615-618) so that target performance parameters will remain within first bound range and second bound range (KR'527: Abstract: Lines 19-27; Col.8 Lines 50-63).

Regarding Claim 20

KR'527 teaches correlating secondary parameters to at least one further secondary parameter (Col.2 Lines 51-63; Col.12 Lines 8-62; Fig.6a-c & 7 a-c).

Regarding Claim 21

KR'527 teaches verifying that all primary and secondary parameters are within allowable limits (Col.13 Lines 24-62).

Regarding Claim 22

HE'277 teaches specifying parameters as first order and second order (HE'277: Col.11 Line 59-Col.12 Line 15).

Regarding Claim 23

Method claim 23 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches determining a set of design distributions that are within a given set of performance targets for a plurality of parameters; altering different features of design; and determining whether altered design is within said set of design distributions (HE'277: Col.5 Line 63-Col.6 Line 24).

Regarding Claim 24

HE'277 teaches developing a product (HE'277: Col.4 Lines 61-Col.5 Line 6) having a device with at least one performance attribute (HE'277: Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15) *wherein the said computer model is generated based on the target model for said transistor* (HE'277: Col.6 Lines 58-62) *and wherein said target model is create using performance parameter for the said performance attribute* (HE'277: Col.5 Lines 40-46). *The goals for device and product are interpreted as same goal, as indicated in the preamble "a product having a device" shows that product only has one device.* HE'277 teaches *target performance parameter includes a first bounded range* (due to process variation being modeled as inequalities - HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34) *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches *said first bounded range comprises performance parameters variations within the single manufacturing process based on a single design for said device* (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34 & 41-60) and; HE'277 teaches said second bounded range *comprises performance parameters variations between designs for said design device (*HE'277: Col.11 Lines 40-Col.12

Line16) as variations in at least the Length and Width of the transistor. In addition claim 24 discloses the "target performance parameter ranges" which HE'277 teaches (HE'277: Col.3 Line 67 – Col.4 Line 40; esp. lines 15-20).

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process *where the performance parameter are current voltage switch point*, although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided as V/I Curves (Abstract: Lines 19-27; Col.8 Lines 50-63). The simulator simulates the computer model, created in the simulator, of the said product to determine if the product/device goals are met (KR'527: Fig.6a-6c).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277:

Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example, **as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 25

Method claim 25 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 26

Method claim 26 discloses similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 27

KR'527 teaches the step of accepting altered device design further comprises the steps of carrying out experiments on test chips (KR'527: Fig.3, actual to simulated data comparison & guard band generation Col.13 Lines 32-62).

Regarding Claim 30 & 33

KR'527 teaches calculating a primary parameter from a physical device feature as L, T and N values (KR'527: Col.11 at least in Lines 19-27); correlating a secondary parameter from said primary parameter as associating resulting I/V curve with the L,

T, N values (KR'527: Col.13 Lines 10-23); *calculating secondary parameter based on the primary parameters based on predetermined primary to secondary correlation I/V curve based on L, T, and N value equation (KR'527: Col.13 Lines 10-23; Fig. 6c; HE'277; Equation 16)*; and comparing said secondary parameter to said target performance parameter (KR'527: Col.13 Lines 24-37).

Regarding Claim 31

KR'527 teaches correlating other secondary parameters from correlations to said secondary parameters as correlating the V/I curve to the various channel length and attributes (short, short long etc) (KR'527: Fig 5a, Element 500).

Regarding Claim 32

KR'527 teaches primary parameter is directly related to physical device feature as related to channel length, doping, gate oxide thickness (KR'527: Col.11 at least in Lines 19-27 & Table C).

Regarding Claim 33

KR'527 teaches correlating primary to secondary parameters (KR'527: Fig 5a, Element 500). Secondary parameters could be derived parameters like "beta" whose derivation using equation is well known in the art.

Regarding Claim 34

Method claim 34 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 35

Method claim 35 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 36

Product claim 36 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product as alternate embodiment (HE'277: Col.22 Lines 1-21).

Regarding Claim 37

Product claim 37 discloses similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 38

Method claim 38 discloses similar limitations as claim 7 and is rejected for the same reasons as claim 7.

Regarding Claim 39

Method claim 39 discloses similar limitations as claim 8 and is rejected for the same reasons as claim 8.

Regarding Claim 40

Method claim 40 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product (storage device) readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method (HE'277: Col.22 Lines 1-21). HE'277 teaches a target model of a device for a product using

the performance parameters for a performance attribute of the said device (HE'277: Col.6 Lines 58-62, Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15), wherein said device is one of a transistor (HE'277: Col.6 Lines 3-6), and wherein said target model comprises a set of subroutines that are adapted to predict process and design variations of said device (HE'277: Col.5 Lines 27-35; Col.6 Lines 1-48). Further, by applicant's own admission such variation predictions softwares are known in the art (Specification: [0033]). HE'277 teaches *target performance parameter includes a first bounded range* (due to process variation being modeled as inequalities - HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34) *and a second bounded range* as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches *said first bounded range comprises performance parameters variations within the single manufacturing process based on a single design for said device* (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34 & 41-60) and; HE'277 teaches said second bounded range *comprises performance parameters variations between designs for said design device* (HE'277: Col.11 Lines 40-Col.12 Line16) as variations in at least the Length and Width of the transistor.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process *where the performance parameter are current voltage switch point (See claim interpretation)*, although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63). The simulator simulates the computer model, created in the simulator, of the said product to determine if the product/device goals are met (KR'527: Fig.6a-6c).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277

discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further applicant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example, **as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

24. Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277 hereafter), in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of applicant's own admission, further in view of U.S. Patent No. 6,028,994 issued to Peng et al (PE'994 hereafter).

Regarding Claim 28 & 29

Teaching of HE'277, KR'527 and applicant's own admission are shown in claim 24 rejections above.

HE'277 & KR'527 do not teach design goals for product, developing product fro from target model and product model simulation & alteration based on feedback.

PE'994 teaches teach design goals for product (PE'994: Col.2 Line 49-59 – predicted performance), developing product from target model as combined product & device model represented by product performance model (PPM) (PE'994: Fig. 1; Col.6 Lines 57-67) and product model simulation & alteration based on feedback as self learning (PE'994: Fig.1 Step 64). The product is represented as package of wafer chip and the device is represented as wafer chip (PE'994: See Fig.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of PE'994 to HE'277 & KR'527. The motivation to combine would have been that HE'277 & KR'527 and PE'994 are attempting to design a model that can mimic and or predict the performance of the semiconductor model (PE'994: Abstract; HE'277 & KR'527: Abstracts) based on the input parameters. Further, teaches PE'994 specifying the

input parameters as ranges (PE'994: Fig.3 Col.5 Lines 35-48) for performance which is very similar to the KR'527 teachings disclosed before relating to ranges for performance parameters.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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